CY7C1441AV33
CY7C1443AV33,CY7C1447AV33

36-Mbit (1M x 36/2M x 18/512K x 72) Flow-Through SRAM

Features

- Supports 133-MHz bus operations
- 1M x 36/2M x 18/512K x 72 common IO
- 3.3V core power supply
- 2.5V or 3.3V IO power supply
- Fast clock-to-output times
  - 6.5 ns (133-MHz version)
- Provide high-performance 2-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- CY7C1441AV33, CY7C1443AV33 available in JEDEC-standard Pb-free 100-pin TQFP package, Pb-free and non-lead-free 165-ball FBGA package. CY7C1447AV33 available in Pb-free and non-lead-free 209-ball FBGA package
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- "ZZ" Sleep Mode option

Functional Description

The CY7C1441AV33/CY7C1443AV33/CY7C1447AV33[1] are 3.3V, 1M x 36/2M x 18/512K x 72 Synchronous Flow-through SRAMs, respectively designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133-MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE_1}$), depth-expansion Chip Enables (CE_2 and $\overline{CE_3}$), Burst Control inputs (ADSC, ADSP, and ADV), Write Enables (BW_x, and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

The CY7C1441AV33/CY7C1443AV33/CY7C1447AV33 allows either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the Processor Address Strobe ($\overline{ADSP}$) or the cache Controller Address Strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the Address Advancement ($\overline{ADV}$) input.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ($\overline{ADV}$).

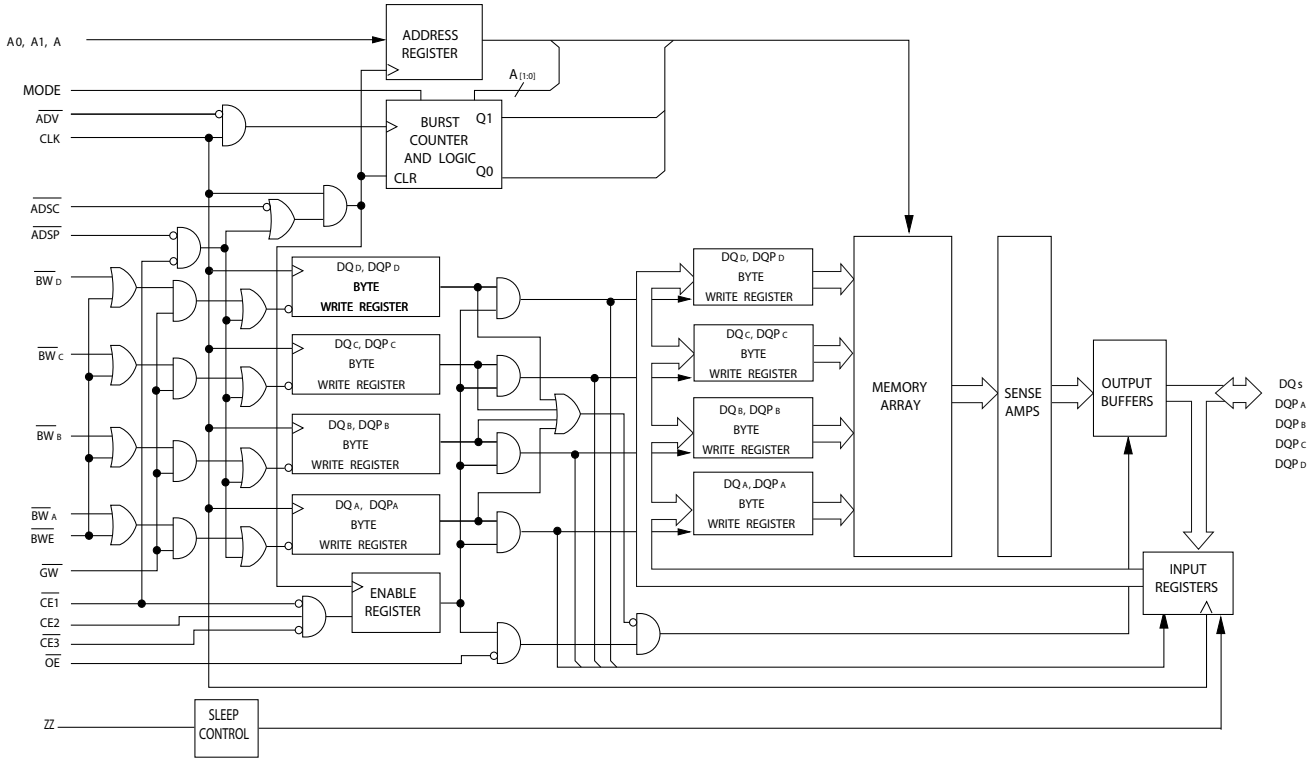
The CY7C1441AV33/CY7C1443AV33/CY7C1447AV33 operates from a +3.3V core power supply while all outputs may operate with either a +2.5 or +3.3V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

Selection Guide

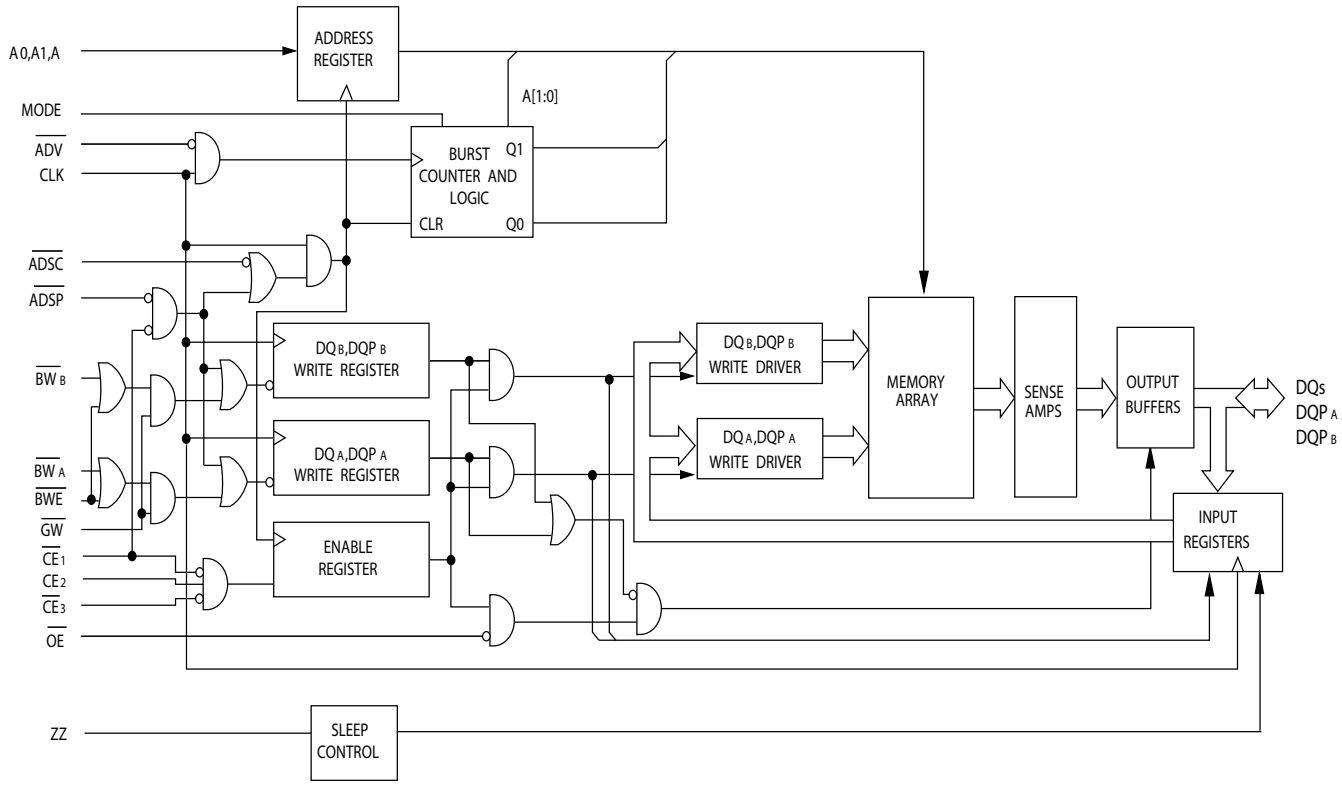
Description	133 MHz	100 MHz	Unit
Maximum Access Time	6.5	8.5	ns
Maximum Operating Current	310	290	mA
Maximum CMOS Standby Current	120	120	mA

Note
1. For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

Logic Block Diagram – CY7C1441AV33 (1M x 36)



Logic Block Diagram – CY7C1443AV33 (2Mx 18)



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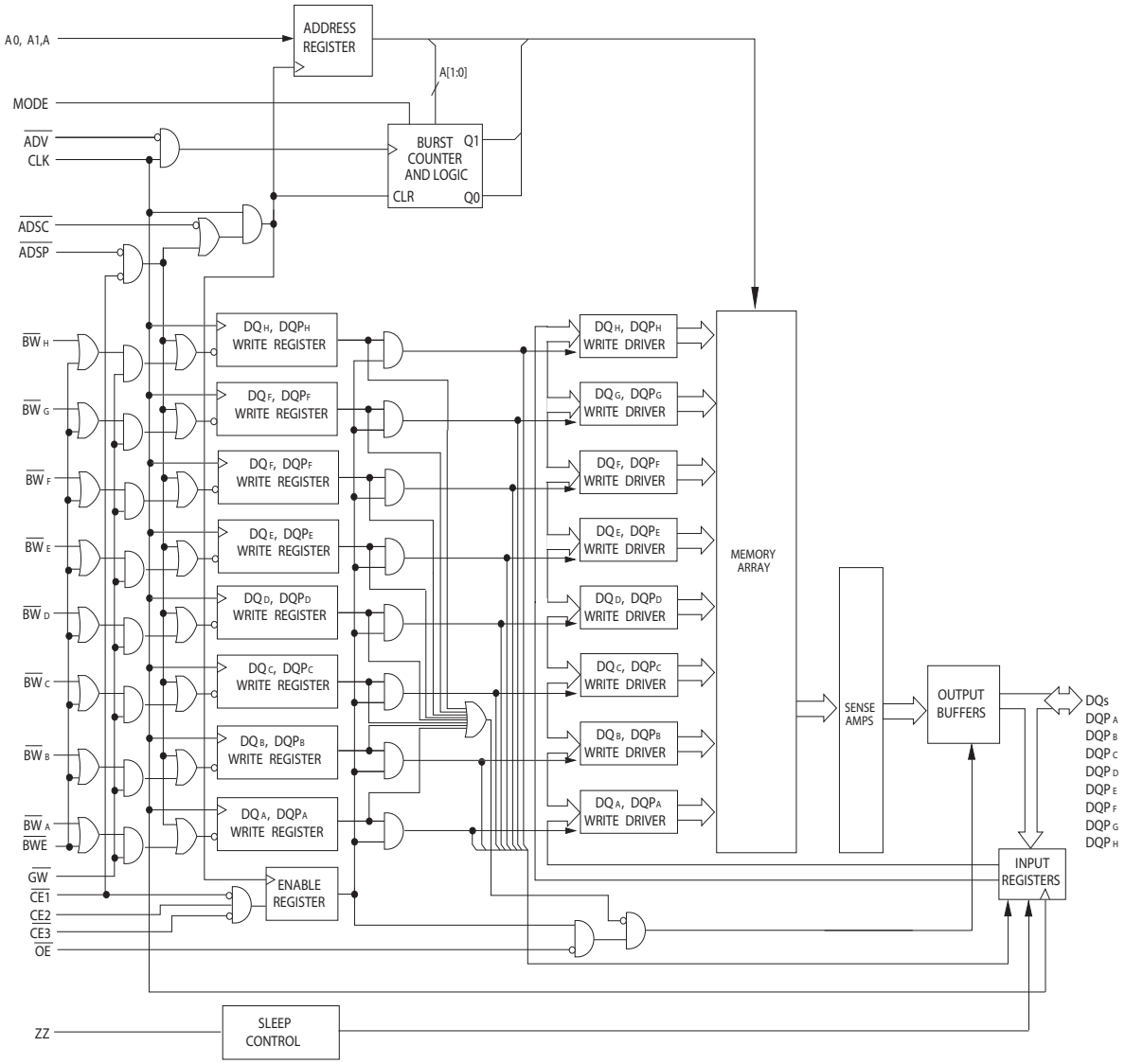
Logic Block Diagram – CY7C1447AV33 (512K x 72)



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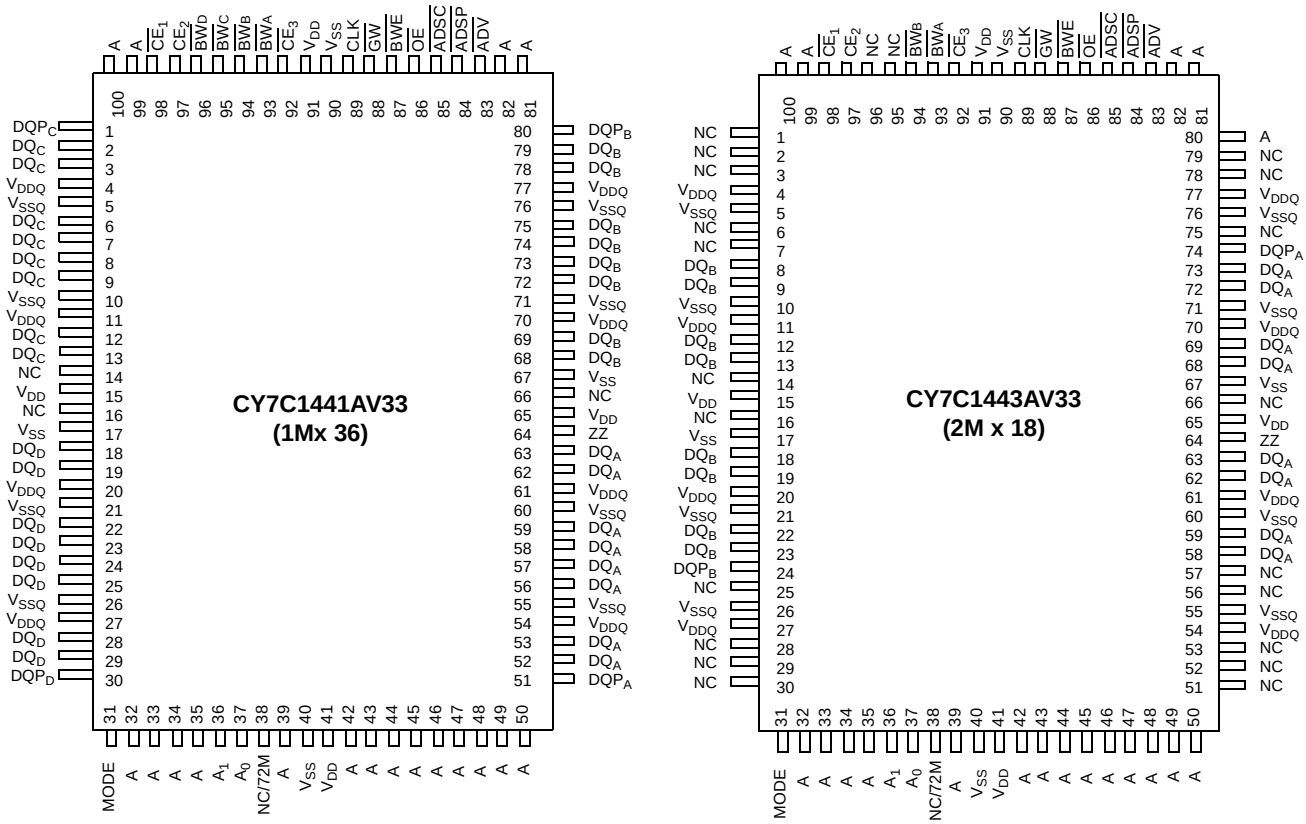
Pin Configurations

Figure 1. 100-Pin TQFP Pinout



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Pin Configurations (continued)

165-ball FBGA (15 x 17 x 1.4 mm) Pinout
CY7C1441AV33 (1M x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC/144M	A	CE_2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

CY7C1443AV33 (2M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
B	NC/144M	A	CE_2	NC	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_A
D	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
E	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
F	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
G	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
K	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
L	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
M	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
N	DQP_B	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

[+] Feedback

Pin Configurations (continued)

209-ball FBGA (14 x 22 x 1.76 mm) Pinout
CY7C1447AV33 (512K × 72)

	1	2	3	4	5	6	7	8	9	10	11
A	DQ_G	DQ_G	A	CE_2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{CE_3}$	A	DQ_B	DQ_B
B	DQ_G	DQ_G	$\overline{BWS_C}$	$\overline{BWS_G}$	NC288M	$\overline{BW}$	A	$\overline{BWS_B}$	$\overline{BWS_F}$	DQ_B	DQ_B
C	DQ_G	DQ_G	$\overline{BWS_H}$	$\overline{BWS_D}$	NC/144M	$\overline{CE_1}$	NC/576M	$\overline{BWS_E}$	$\overline{BWS_A}$	DQ_B	DQ_B
D	DQ_G	DQ_G	V_{SS}	NC	NC/1G	$\overline{OE}$	$\overline{GW}$	NC	V_{SS}	DQ_B	DQ_B
E	DQP_G	DQP_C	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQP_F	DQP_B
F	DQ_C	DQ_C	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQ_F	DQ_F
G	DQ_C	DQ_C	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_F	DQ_F
H	DQ_C	DQ_C	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQ_F	DQ_F
J	DQ_C	DQ_C	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_F	DQ_F
K	NC	NC	CLK	NC	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC	NC
L	DQ_H	DQ_H	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_A	DQ_A
M	DQ_H	DQ_H	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQ_A	DQ_A
N	DQ_H	DQ_H	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_A	DQ_A
P	DQ_H	DQ_H	V_{SS}	V_{SS}	V_{SS}	ZZ	V_{SS}	V_{SS}	V_{SS}	DQ_A	DQ_A
R	DQP_D	DQP_H	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQP_A	DQP_E
T	DQ_D	DQ_D	V_{SS}	NC	NC	MODE	NC	NC	V_{SS}	DQ_E	DQ_E
U	DQ_D	DQ_D	NC/72M	A	A	A	A	A	A	DQ_E	DQ_E
V	DQ_D	DQ_D	A	A	A	A1	A	A	A	DQ_E	DQ_E
W	DQ_D	DQ_D	TMS	TDI	A	A0	A	TDO	TCK	DQ_E	DQ_E

[+] Feedback

Pin Definitions

Name	IO	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs Used to Select One of the Address Location**s. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$ $\overline{BW}_C$, $\overline{BW}_D$, $\overline{BW}_E$, $\overline{BW}_F$, BW_G, BW_H	Input-Synchronous	**Byte Write Select Inputs, Active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global Write Enable Input, Active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on BW_X and $\overline{BWE}$).
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device. ADSP is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device. $\overline{CE}_3$ is assumed active throughout this document for BGA. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Asynchronous Input, Active LOW**. Controls the direction of the IO pins. When LOW, the IO pins behave as outputs. When deasserted HIGH, IO pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance Input Signal, Sampled on the Rising Edge of CLK**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address Strobe from Processor, Sampled on the Rising Edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH
$\overline{ADSC}$	Input-Synchronous	**Address Strobe from Controller, Sampled on the Rising Edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized·
$\overline{BWE}$	Input-Synchronous	**Byte Write Enable Input, Active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
ZZ	Input-Asynchronous	**ZZ "sleep" Input, Active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull down.

[+] Feedback

Pin Definitions (continued)

Name	IO	Description
DQ_s	IO-Synchronous	**Bidirectional Data IO lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_s and DQP_X are placed in a tri-state condition.The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	IO-Synchronous	**Bidirectional Data Parity IO Lines.** Functionally, these signals are identical to DQ_s. During write sequences, DQP_x is controlled by $BW_{[A:H]}$ correspondingly.
MODE	Input-Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull up.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{DDQ}	IO Power Supply	**Power Supply for the IO Circuitry**.
V_{SS}	Ground	**Ground for the Core of the Device**.
V_{SSQ}	IO Ground	**Ground for the IO Circuitry**.
TDO	JTAG serial output Synchronous	**Serial Data-Out to the JTAG Circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not being utilized, this pin should be left unconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input Synchronous	**Serial Data-In to the JTAG Circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be left floating or connected to V_{DD} through a pull up resistor. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	**Serial Data-In to the JTAG Circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG-Clock	**Clock Input to the JTAG Circuitry**. If the JTAG feature is not being utilized, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	-	**No Connects**. Not internally connected to the die. 72M, 144M and 288M are address expansion pins are not internally connected to the die.
NC/72M, NC/144M, NC/288M, NC/576M NC/1G	-	**No Connects**. Not internally connected to the die. NC/72M, NC/144M, NC/288M, NC/576M and NC/1G are address expansion pins are not internally connected to the die.

[+] Feedback

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133-MHz device).

The CY7C1441AV33/CY7C1443AV33/CY7C1447AV33 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select (BW_X) inputs. A Global Write Enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. ADSP is ignored if $\overline{CE_1}$ is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, and (2) ADSP or ADSC is asserted LOW (if the access is initiated by ADSC, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the $\overline{OE}$ input is asserted LOW, the requested data is available at the data outputs a maximum to t_{CDV} after clock rise. ADSP is ignored if $\overline{CE_1}$ is HIGH.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, CE_2, $\overline{CE_3}$ are all asserted active, and (2) ADSP is asserted LOW. The addresses presented are loaded into the address register and the burst inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$)are ignored during this first clock cycle. If the write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a write) on the next clock rise, the appropriate data is latched and written into the device. Byte writes are allowed. All IOs are tri-stated during a byte write.Since this is a common IO device, the asynchronous $\overline{OE}$ input signal must be deasserted and the IOs must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, (2) ADSC is asserted LOW, (3) ADSP is deasserted HIGH, and (4) the write input signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) indicate a write access. ADSC is ignored if ADSP is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to DQ_S is written into the specified address location. Byte writes are allowed. All IOs are tri-stated when a write is detected, even a byte write. Since this is a common IO device, the asynchronous $\overline{OE}$ input signal must be deasserted and the IOs must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1441AV33/CY7C1443AV33/CY7C1447AV33 provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE selects a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE_1}$, CE_2, $\overline{CE_3}$, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

[+] Feedback

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Sleep mode standby current	ZZ ≥ V_{DD} – 0.2V		100	mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ V_{DD} – 0.2V		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2V	$2t_{CYC}$		ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0		ns

Truth Table

tThe truth table for CY7C1441AV33/CY7C1443AV33/CY7C1447AV33 follows.[2, 3, 4, 5, 6]

Cycle Description	ADDRESS Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-State
Deselected Cycle, Power down	None	L	L	X	L	L	X	X	X	X	L-H	Tri-State
Deselected Cycle, Power down	None	L	X	H	L	L	X	X	X	X	L-H	Tri-State
Deselected Cycle, Power down	None	L	L	X	L	H	L	X	X	X	L-H	Tri-State
Deselected Cycle, Power down	None	X	X	X	L	H	L	X	X	X	L-H	Tri-State
Sleep Mode, Power down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Tri-State
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-State
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-State
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-State
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Notes
2. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
3. $\overline{WRITE}$ = L when any one or more Byte Write enable signals and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
4. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
6. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

[+] Feedback

Partial Truth Table for Read/Write

Function (CY7C1441AV33)[2, 7]	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A (DQ_A, DQP_A)	H	L	H	H	H	L
Write Byte B(DQ_B, DQP_B)	H	L	H	H	L	H
Write Bytes A, B (DQ_A, DQ_B, DQP_A, DQP_B)	H	L	H	H	L	L
Write Byte C (DQ_C, DQP_C)	H	L	H	L	H	H
Write Bytes C, A (DQ_C, DQ_A, DQP_C, DQP_A)	H	L	H	L	H	L
Write Bytes C, B (DQ_C, DQ_B, DQP_C, DQP_B)	H	L	H	L	L	H
Write Bytes C, B, A (DQ_C, DQ_B, DQ_A, DQP_C, DQP_B, DQP_A)	H	L	H	L	L	L
Write Byte D (DQ_D, DQP_D)	H	L	L	H	H	H
Write Bytes D, A (DQ_D, DQ_A, DQP_D, DQP_A)	H	L	L	H	H	L
Write Bytes D, B (DQ_D, DQ_A, DQP_D, DQP_A)	H	L	L	H	L	H
Write Bytes D, B, A (DQ_D, DQ_B, DQ_A, DQP_D, DQP_B, DQP_A)	H	L	L	H	L	L
Write Bytes D, B (DQ_D, DQ_B, DQP_D, DQP_B)	H	L	L	L	H	H
Write Bytes D, B, A (DQ_D, DQ_C, DQ_A, DQP_D, DQP_C, DQP_A)	H	L	L	L	H	L
Write Bytes D, C, A (DQ_D, DQ_B, DQ_A, DQP_D, DQP_B, DQP_A)	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Truth Table for Read/Write

Function (CY7C1443AV33)[2]	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte A - (DQ_A and DQP_A)	H	L	H	L
Write Byte B - (DQ_B and DQP_B)	H	L	L	H
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

Truth Table for Read/Write

Function (CY7C1447AV33)[2, 8]	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_X}$
Read	H	H	X
Read	H	L	All $\overline{BW}$ = H
Write Byte x – (DQ_X and DQP_X)	H	L	L
Write All Bytes	H	L	All $\overline{BW}$ = L
Write All Bytes	L	X	X

Notes
7. Table only lists a partial listing of the byte write combinations. Any Combination of $\overline{BW_X}$ is valid Appropriate write is done based on which byte write is active.
8. BWx represents any byte write signal $\overline{BW_{[A:H]}}$.To enable any byte write $\overline{BW_x}$, a Logic LOW signal should be applied at clock rise.Any number of bye writes can be enabled at the same time for any given write.

[+] Feedback

IEEE 1149.1 Serial Boundary Scan (JTAG)

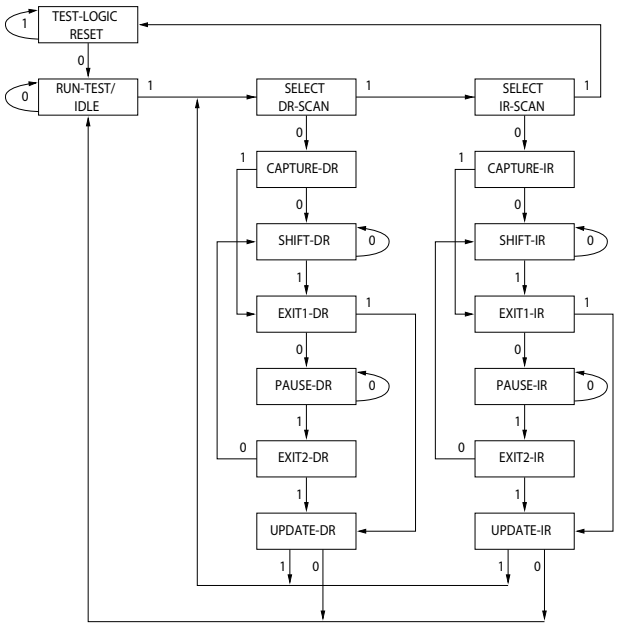
The CY7C1441AV33/CY7C1443AV33/CY7C1447AV33 incorporates a serial boundary scan test access port (TAP). This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 3.3V or 2.5V IO logic levels.

The CY7C1441AV33/CY7C1443AV33/CY7C1447AV33 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull up resistor. TDO should be left unconnected. Upon power up, the device comes up in a reset state which does not interfere with the operation of the device.

TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

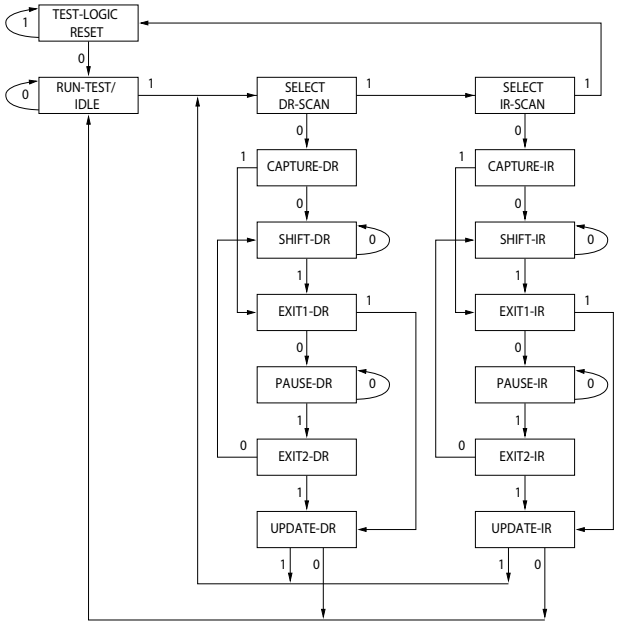
Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Tap Controller Block Diagram.)

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Tap Controller State Diagram.)

TAP Controller State Diagram



Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and scan data into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

[+] Feedback

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the Tap Controller Block Diagram. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This shifts data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM IO ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the IO ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO balls and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High-Z state until the next command is given during the “Update IR” state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required—that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

[+] Feedback

EXTEST

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the shift-DR controller state.

EXTEST OUTPUT BUS TRI-STATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

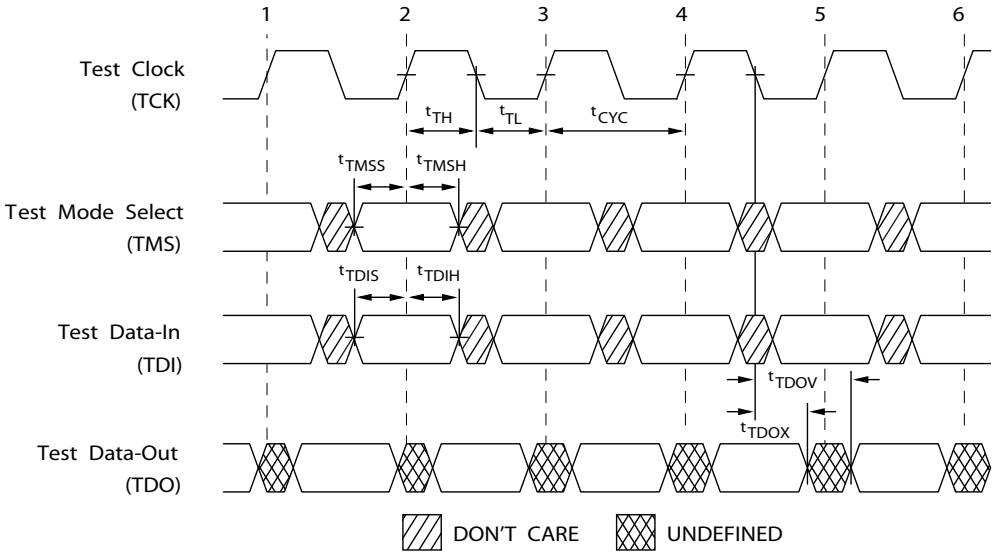
The boundary scan register has a special bit located at bit #89 (for 165-FBGA package) or bit #138 (for 209-FBGA package). When this scan cell, called the “extest output bus tri-state”, is latched into the preload register during the “Update-DR” state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High-Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the “Shift-DR” state. During “Update-DR”, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is pre-set HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the “Test-Logic-Reset” state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Timing



[+] Feedback

TAP AC Switching Characteristics

Over the Operating Range[9, 10]

Parameter	Description	Min.	Max.	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH time	20		ns
t_{TL}	TCK Clock LOW time	20		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5		ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5		ns
t_{CS}	Capture Setup to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns

Notes
9. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
10. Test conditions are specified using the load in TAP AC test Conditions. t_R/t_F = 1 ns.

[+] Feedback

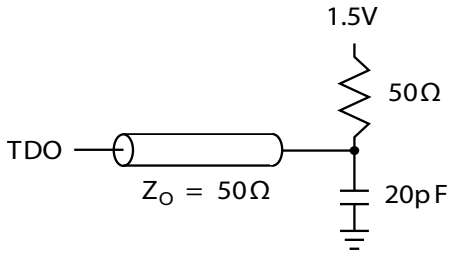
3.3V TAP AC Test Conditions

Input pulse levels.....V_{SS} to 3.3V
Input rise and fall times.....1 ns
Input timing reference levels.....1.5V
Output reference levels 1.5V
Test load termination supply voltage 1.5V

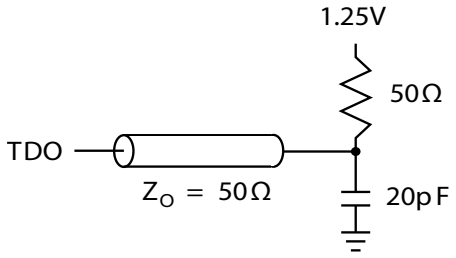
2.5V TAP AC Test Conditions

Input pulse levels.....V_{SS} to 2.5V
Input rise and fall time .....1 ns
Input timing reference levels.....1.25V
Output reference levels 1.25V
Test load termination supply voltage 1.25V

3.3V TAP AC Output Load Equivalent



2.5V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics And Operating Conditions

(0°C < TA < +70°C; V_{DD} = 3.135V to 3.6V unless otherwise noted)[11]

Parameter	Description	Description	Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA	V_{DDQ} = 3.3V	2.4		V
		I_{OH} = –1.0 mA	V_{DDQ} = 2.5V	2.0		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3V	2.9		V
			V_{DDQ} = 2.5V	2.1		V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA	V_{DDQ} = 3.3V		0.4	V
		I_{OL} = 1.0 mA	V_{DDQ} = 2.5V		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3V		0.2	V
			V_{DDQ} = 2.5V		0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 3.3V	2.0	V_{DD} + 0.3	V
			V_{DDQ} = 2.5V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 3.3V	–0.3	0.8	V
			V_{DDQ} = 2.5V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Note
11. All voltages referenced to V_{SS} (GND).

[+] Feedback

Identification Register Definitions

Instruction Field	CY7C1441AV33 (1M x 36)	CY7C1443AV33 (2M x 18)	CY7C1447AV33 (512K x 72)	Description
Revision Number (31:29)	000	000	000	Describes the version number.
Device Depth (28:24)	01011	01011	01011	Reserved for Internal Use
Architecture/Memory Type(23:18)[12]	000001	000001	000001	Defines memory type and architecture
Bus Width/Density(17:12)	100111	010111	110111	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (x36)	Bit Size (x18)	Bit Size (x18)
Instruction	3	3	3
Bypass	1	1	1
ID	32	32	32
Boundary Scan Order (165-ball FBGA package)	89	89	-
Boundary Scan Order (209-ball FBGA package)	-	-	138

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures IO ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Note
12. Bit #24 is “1” in the ID Register Definitions for both 2.5V and 3.3V versions of this device.

165-ball FBGA Boundary Scan Order[13,14]

CY7C1441AV33 (1M x 36), CY7C1443AV33 (2M x 18)

Bit #	Ball ID	Bit #	Ball ID	Bit #	Ball ID	Bit #	Ball ID
1	N6	26	E11	51	A3	76	N1
2	N7	27	D11	52	A2	77	N2
3	N10	28	G10	53	B2	78	P1
4	P11	29	F10	54	C2	79	R1
5	P8	30	E10	55	B1	80	R2
6	R8	31	D10	56	A1	81	P3
7	R9	32	C11	57	C1	82	R3
8	P9	33	A11	58	D1	83	P2
9	P10	34	B11	59	E1	84	R4
10	R10	35	A10	60	F1	85	P4
11	R11	36	B10	61	G1	86	N5
12	H11	37	A9	62	D2	87	P6
13	N11	38	B9	63	E2	88	R6
14	M11	39	C10	64	F2	89	Internal
15	L11	40	A8	65	G2		
16	K11	41	B8	66	H1		
17	J11	42	A7	67	H3		
18	M10	43	B7	68	J1		
19	L10	44	B6	69	K1		
20	K10	45	A6	70	L1		
21	J10	46	B5	71	M1		
22	H9	47	A5	72	J2		
23	H10	48	A4	73	K2		
24	G11	49	B4	74	L2		
25	F11	50	B3	75	M2		

Notes
13. Balls which are NC (No Connect) are preset LOW.
14. Bit# 89 is preset HIGH.

[+] Feedback

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND .....–0.3V to +4.6V

Supply Voltage on V_{DDQ} Relative to GND..... –0.3V to +V_{DD}

DC Voltage Applied to Outputs in Tri-State .....–0.5V to V_{DDQ} + 0.5V

DC Input Voltage .....–0.5V to V_{DD} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V –5%/+10%	2.5V –5% to V_{DD}
Industrial	–40°C to +85°C		

Electrical Characteristics Over the Operating Range[15, 16]

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	IO Supply Voltage	for 3.3V IO		3.135	V_{DD}	V
		for 2.5V IO		2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3V IO, I_{OH} = –4.0 mA		2.4		V
		for 2.5V IO, I_{OH} = –1.0 mA		2.0		V
V_{OL}	Output LOW Voltage	for 3.3V IO, I_{OL} = 8.0 mA			0.4	V
		for 2.5V IO, I_{OL} = 1.0 mA			0.4	V
V_{IH}	Input HIGH Voltage[15]	for 3.3V IO		2.0	V_{DD} + 0.3V	V
		for 2.5V IO		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[15]	for 3.3V IO		–0.3	0.8	V
		for 2.5V IO		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	7.5-ns cycle, 133 MHz		310	mA
			10-ns cycle, 100 MHz		290	mA
I_{SB1}	Automatic CE Power down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}, inputs switching	All Speeds		180	mA
I_{SB2}	Automatic CE Power down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{DD} – 0.3V or V_{IN} ≤ 0.3V, f = 0, inputs static	All speeds		120	mA
I_{SB3}	Automatic CE Power down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{DDQ} – 0.3V or V_{IN} ≤ 0.3V, f = f_{MAX}, inputs switching	All Speeds		180	mA
I_{SB4}	Automatic CE Power down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{DD} – 0.3V or V_{IN} ≤ 0.3V, f = 0, inputs static	All Speeds		135	mA

Notes

15. Overshoot: V_{IH}(AC) < V_{DD} +1.5V (Pulse width less than t_{CYC}/2), undershoot: V_{IL}(AC) > –2V (Pulse width less than t_{CYC}/2).
16. $T_{Power\text{-}up}$: Assumes a linear ramp from 0V to V_{DD}(min.) within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

[+] Feedback

Capacitance

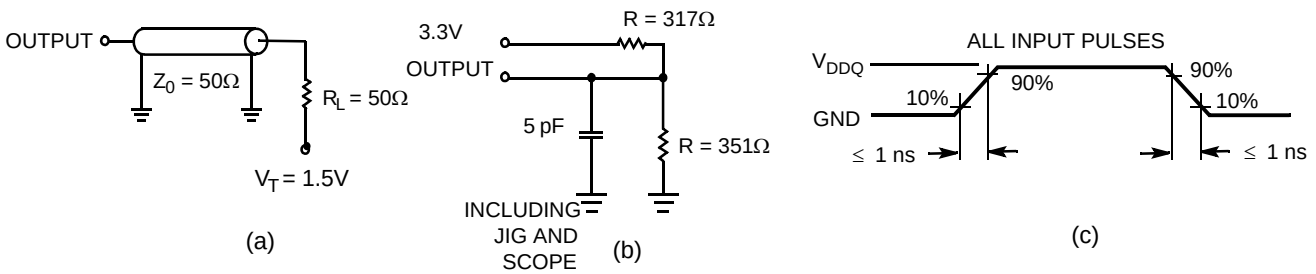
Parameter[17]	Description	Test Conditions	100 TQFP Max.	165 FBGA Max.	209 FBGA Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V V_{DDQ} = 2.5V	6.5	7	5	pF
C_{CLK}	Clock Input Capacitance		3	7	5	pF
C_{IO}	Input/Output Capacitance		5.5	6	7	pF

Thermal Resistance

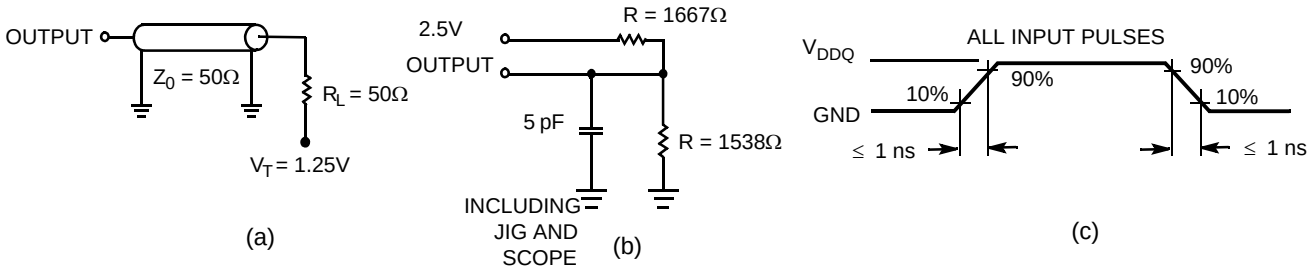
Parameter[17]	Description	Test Conditions	100 TQFP Package	165 FBGA Package	209 FBGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	25.21	20.8	25.31	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		2.28	3.2	4.48	°C/W

Figure 2. AC Test Loads and Waveforms

3.3V IO Test Load



2.5V IO Test Load



Note
17. Tested initially and after any design or process change that may affect these parameters

[+] Feedback

Switching Characteristics

Over the Operating Range[22, 23]

Parameter	Description	–133		–100		Unit
		Min.	Max.	Min.	Max.	
t_{POWER}	V_{DD} (Typical) to the first Access[18]	1		1		ms
Clock						
t_{CYC}	Clock Cycle Time	7.5		10		ns
t_{CH}	Clock HIGH	2.5		3.0		ns
t_{CL}	Clock LOW	2.5		3.0		ns
Output Times						
t_{CDV}	Data Output Valid After CLK Rise		6.5		8.5	ns
t_{DOH}	Data Output Hold After CLK Rise	2.5		2.5		ns
t_{CLZ}	Clock to Low-Z[19, 20, 21]	2.5		2.5		ns
t_{CHZ}	Clock to High-Z[19, 20, 21]		3.8	0	4.5	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid		3.0		3.8	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low-Z[19, 20, 21]	0		0		ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High-Z[19, 20, 21]		3.0		4.0	ns
Setup Times						
t_{AS}	Address Setup Before CLK Rise	1.5		1.5		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Setup Before CLK Rise	1.5		1.5		ns
t_{ADVS}	$\overline{ADV}$ Setup Before CLK Rise	1.5		1.5		ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Setup Before CLK Rise	1.5		1.5		ns
t_{DS}	Data Input Setup Before CLK Rise	1.5		1.5		ns
t_{CES}	Chip Enable Setup	1.5		1.5		ns
Hold Times						
t_{AH}	Address Hold After CLK Rise	0.5		0.5		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Hold After CLK Rise	0.5		0.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		ns

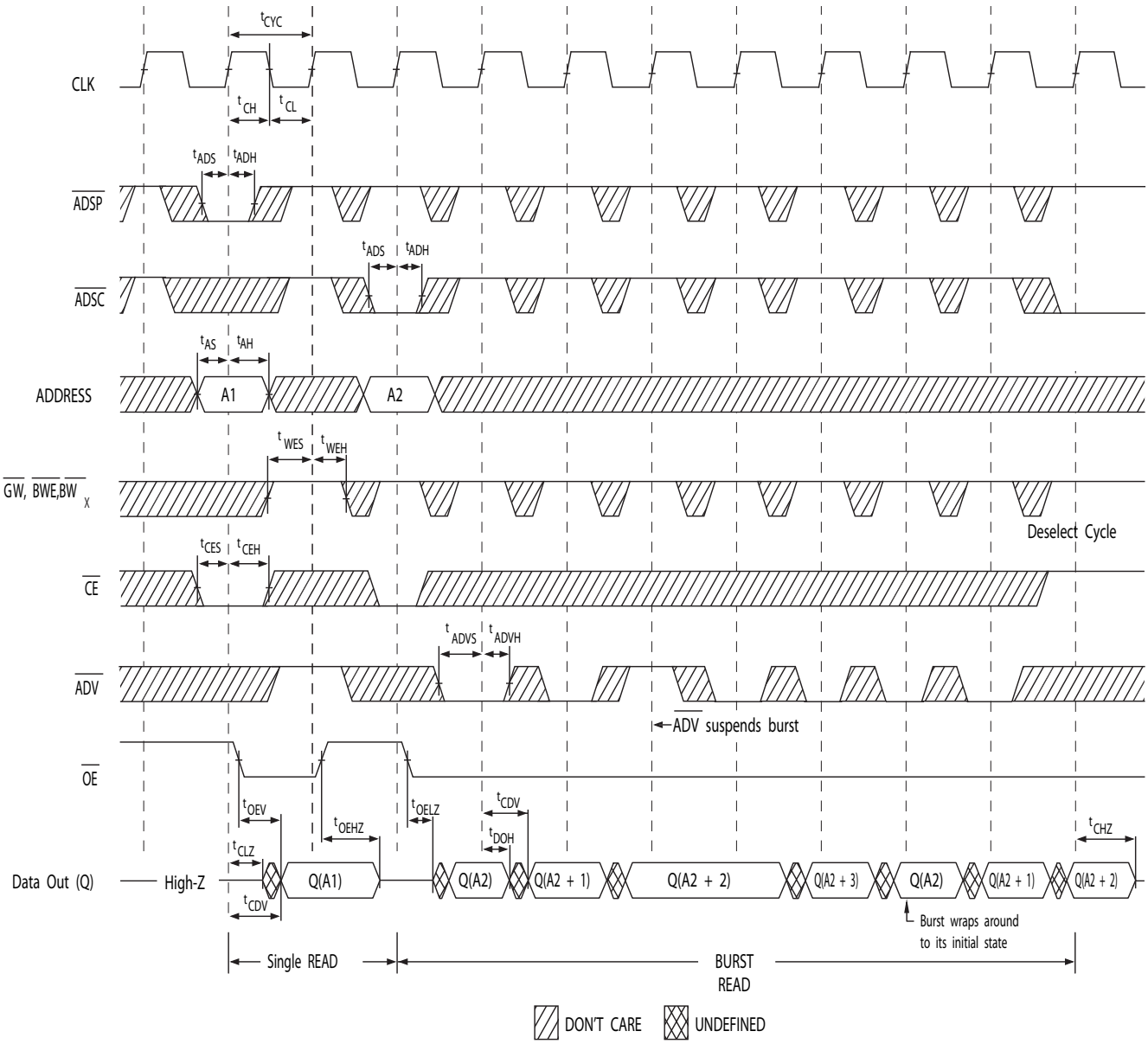
Notes

18. This part has a voltage regulator internally; t_{POWER} is the time that the power must be supplied above V_{DD}(minimum) initially, before a read or write operation can be initiated.
19. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of "AC Test Loads and Waveforms" on page 20. Transition is measured ± 200 mV from steady-state voltage.
20. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
21. This parameter is sampled and not 100% tested.
22. Timing reference level is 1.5V when V_{DDQ} = 3.3V and is 1.25V when V_{DDQ} = 2.5V.
23. Test conditions shown in (a) of AC Test Loads unless otherwise noted.

[+] Feedback

Timing Diagrams

Figure 3. Read Cycle Timing[24]



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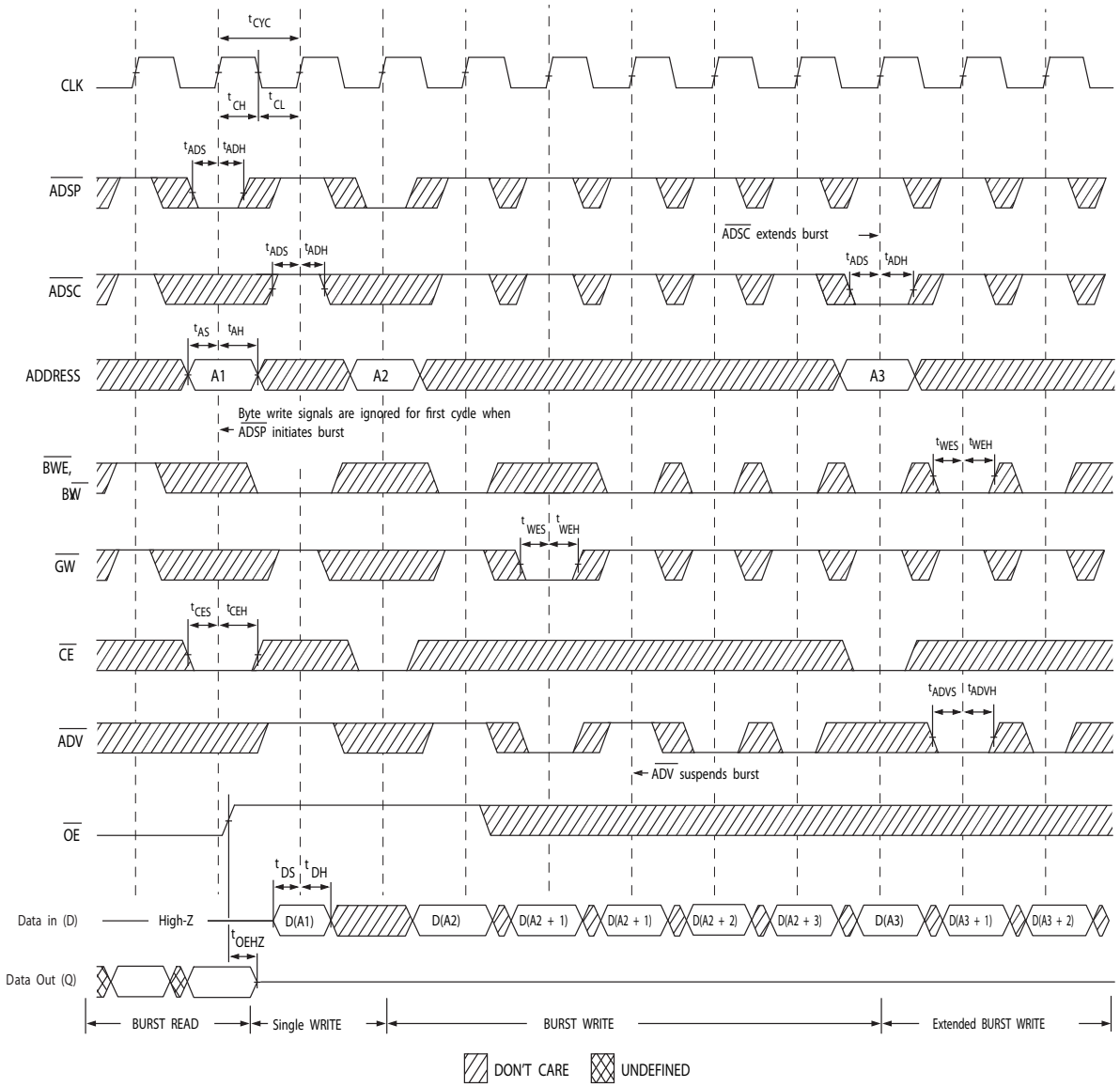
Note
24. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

[+] Feedback

Timing Diagrams (continued)

Figure 4. Write Cycle Timing[24, 25]



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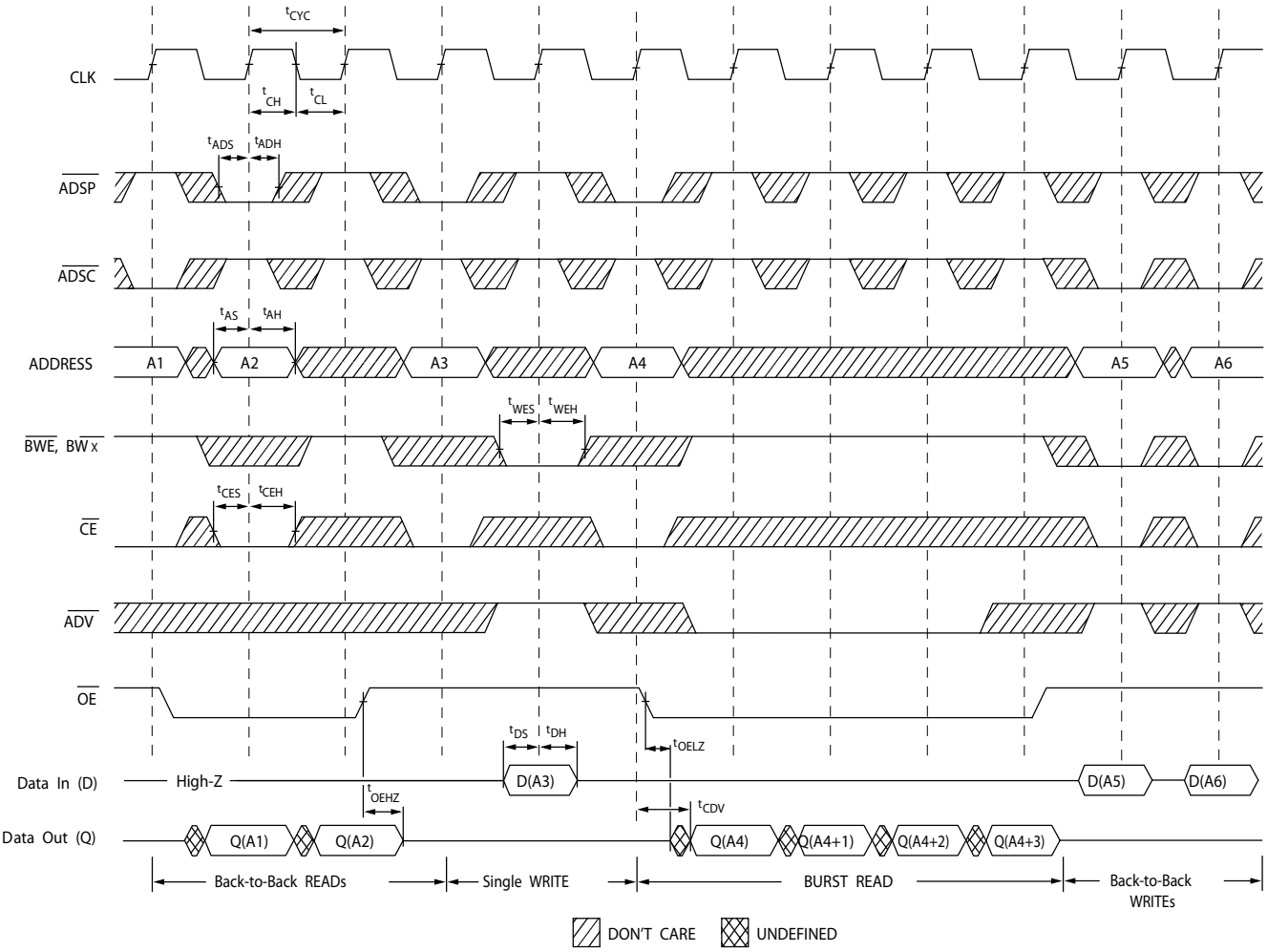
Note
25. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_X$ LOW

[+] Feedback

Timing Diagrams (continued)

Figure 5. Read/Write Cycle Timing[24, 26, 27]



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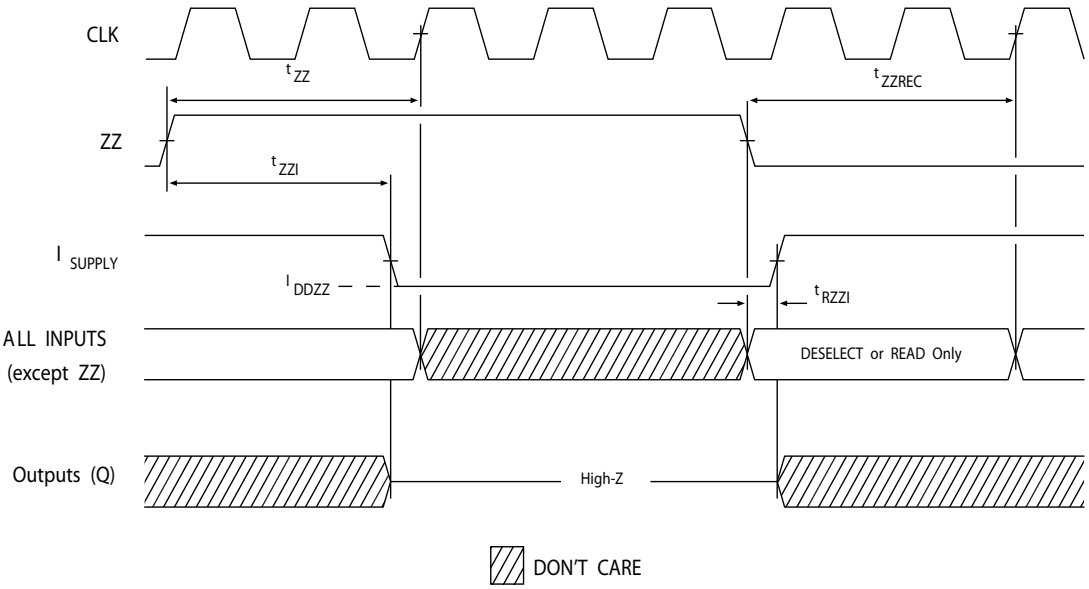
Note
26. The data bus (Q) remains in high-Z following a WRITE cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
27. $\overline{GW}$ is HIGH

[+] Feedback

Timing Diagrams (continued)

Figure 6. ZZ Mode Timing[28, 29]



Note
28. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
29. DQs are in high-Z when exiting ZZ sleep mode.

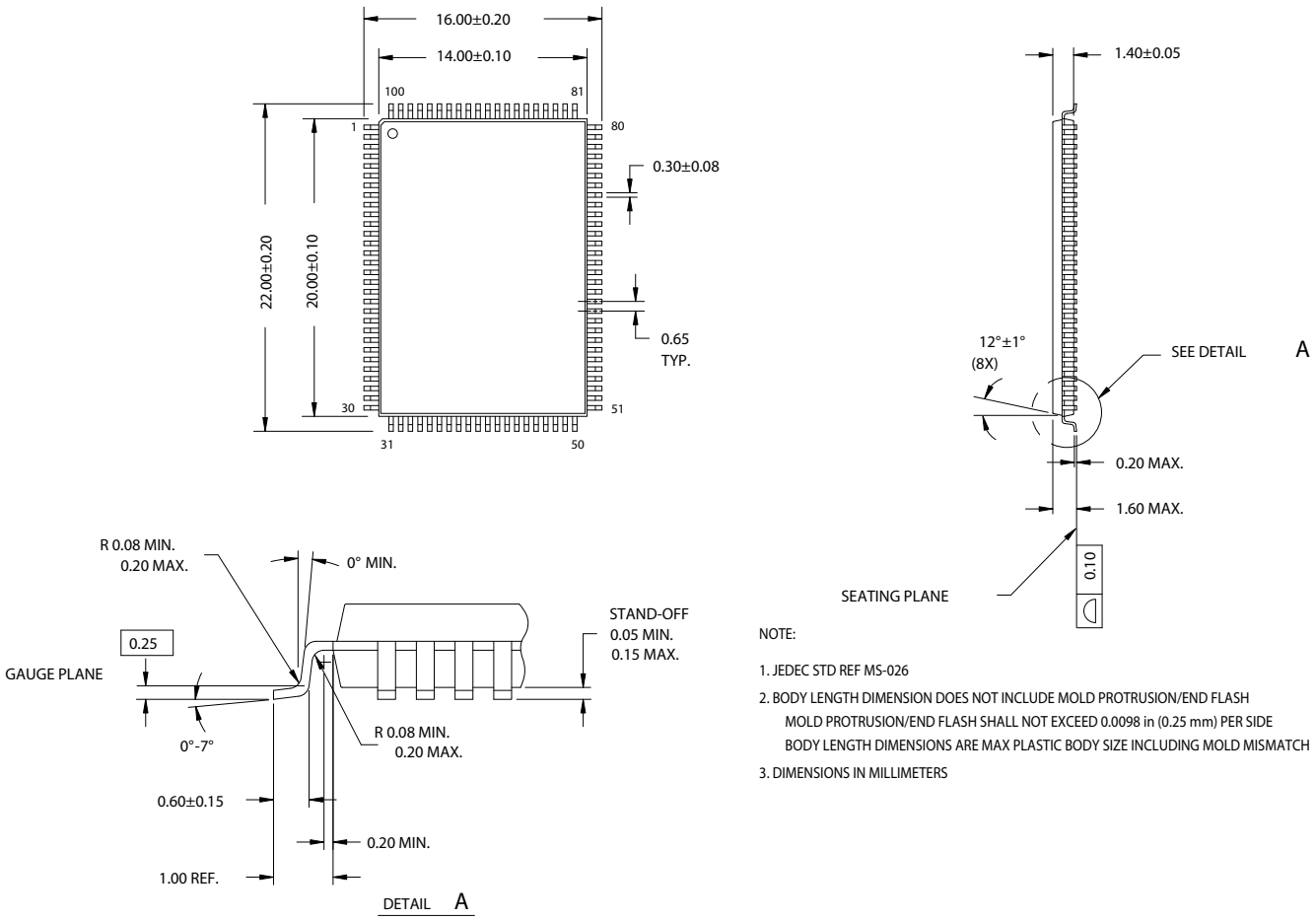
Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1441AV33-133AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-free	Commercial
	CY7C1443AV33-133AXC			
	CY7C1441AV33-133BZC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1443AV33-133BZC			
	CY7C1441AV33-133BZXC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-free	
	CY7C1443AV33-133BZXC			
	CY7C1447AV33-133BGC	51-85167	209-ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm)	
	CY7C1447AV33-133BGXC		209-ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm) Pb-free	
	CY7C1441AV33-133AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-free	Industrial
	CY7C1443AV33-133AXI			
	CY7C1441AV33-133BZI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1443AV33-133BZI			
	CY7C1441AV33-133BZXI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-free	
	CY7C1443AV33-133BZXI			
	CY7C1447AV33-133BGI	51-85167	209-ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm)	
	CY7C1447AV33-133BGXI		209-ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm) Pb-free	
100	CY7C1441AV33-100AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-free	Commercial
	CY7C1443AV33-100AXC			
	CY7C1441AV33-100BZC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1443AV33-100BZC			
	CY7C1441AV33-100BZXC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-free	
	CY7C1443AV33-100BZXC			
	CY7C1447AV33-100BGC	51-85167	209-ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm)	
	CY7C1447AV33-100BGXC		209-ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm) Pb-free	
	CY7C1441AV33-100AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-free	Industrial
	CY7C1443AV33-100AXI			
	CY7C1441AV33-100BZI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1443AV33-100BZI			
	CY7C1441AV33-100BZXI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-free	
	CY7C1443AV33-100BZXI			
	CY7C1447AV33-100BGI	51-85167	209-ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm)	
	CY7C1447AV33-100BGXI		209-ball Fine-Pitch Ball Grid Array (14 x 22 x 1.76 mm) Pb-free	

Package Diagrams

Figure 1. 100-pin TQFP (14 x 20 x 1.4 mm) (51-85050)



NOTE:

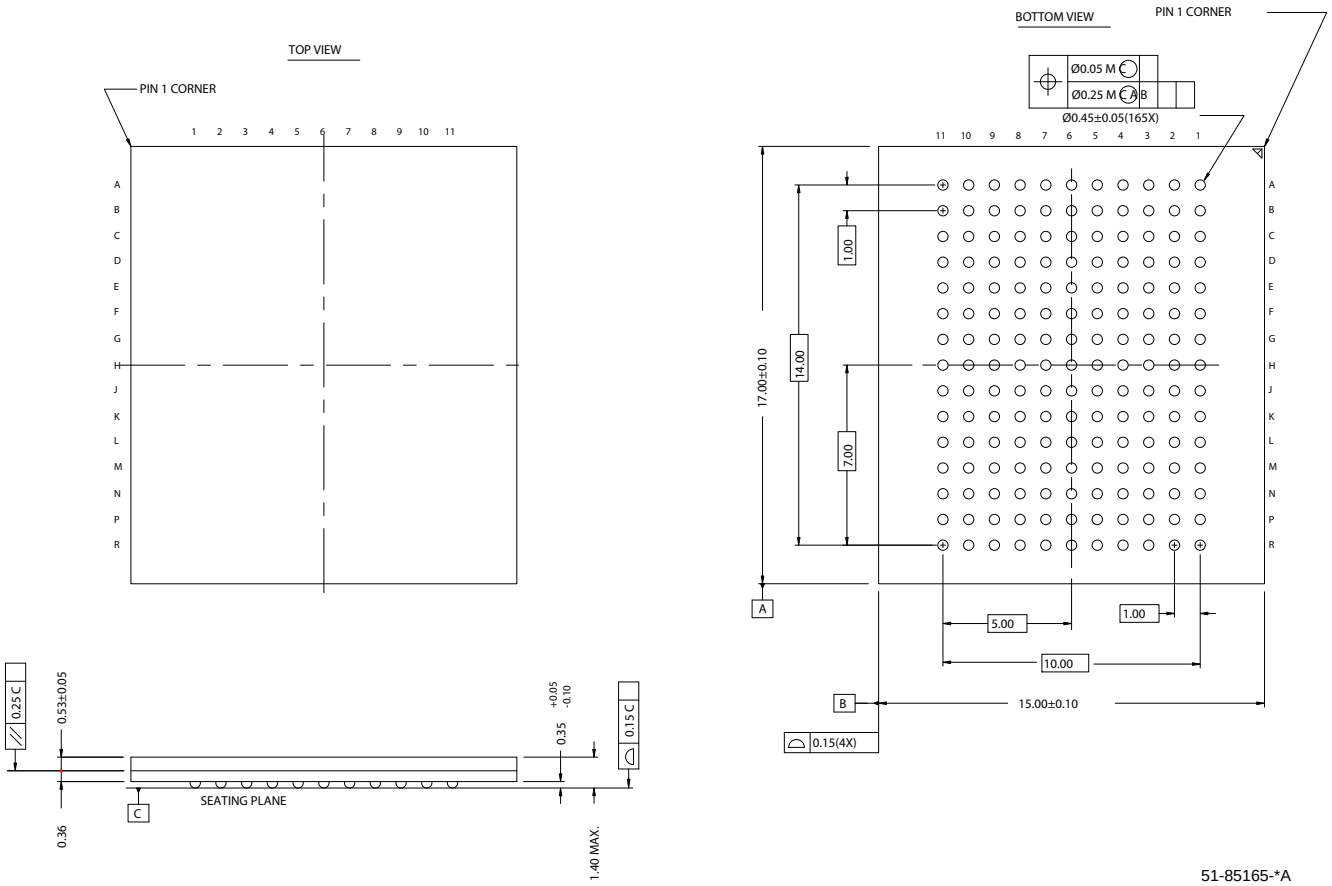
1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050-*B

[+] Feedback

Package Diagrams (continued)

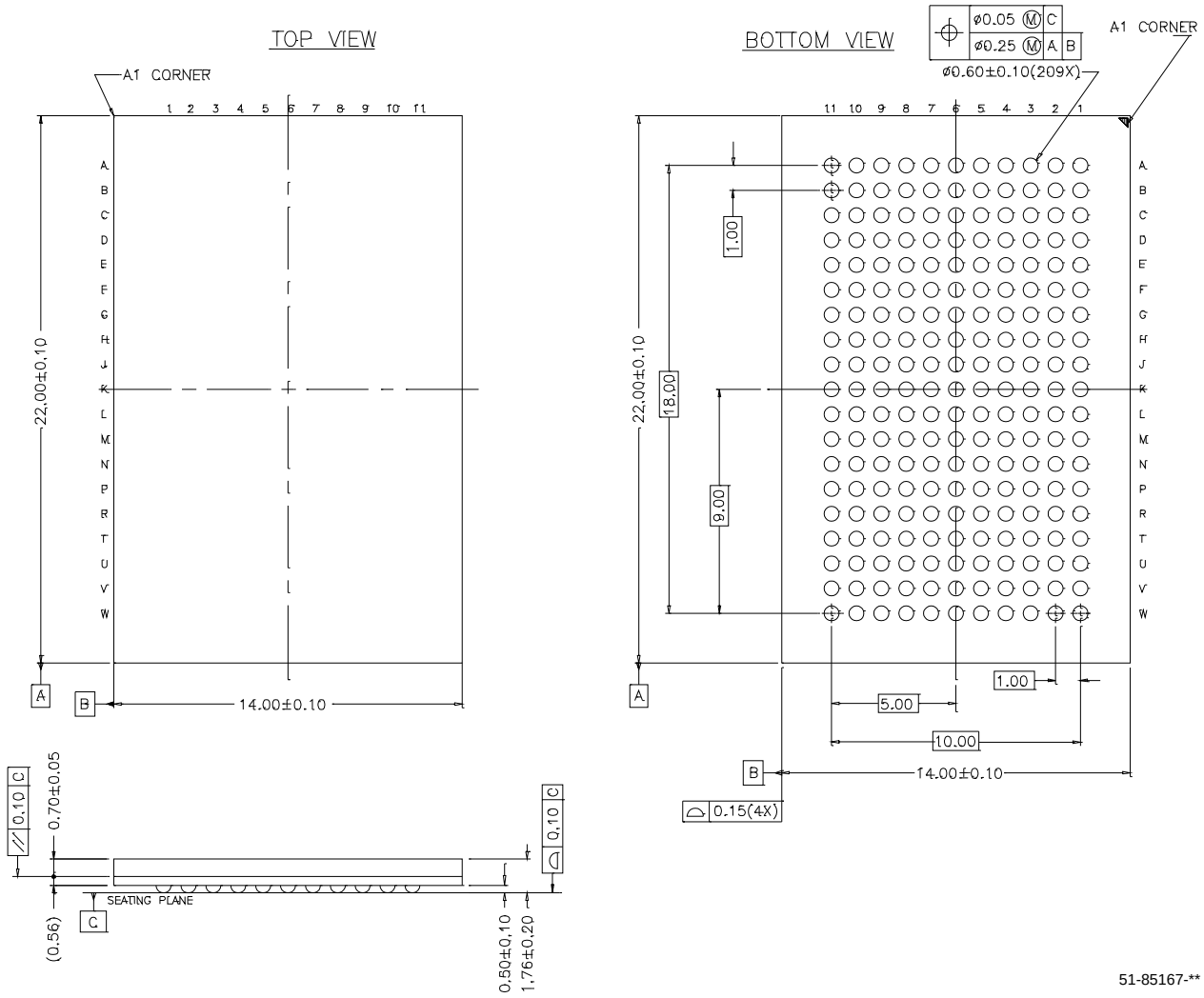
Figure 2. 165-ball FBGA (15 x 17 x 1.4 mm) (51-85165)



[+] Feedback

Package Diagrams (continued)

Figure 3. 209-ball FBGA (14 x 22 x1.76 mm) (51-85167)



[+] Feedback

Document History Page

Document Title: CY7C1441AV33/CY7C1443AV33/CY7C1447AV33 36-Mbit (1M x 36/2M x 18/512K x 72) Flow-Through SRAM Document Number: 38-05357				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	124459	03/06/03	CJM	New Data Sheet
*A	254910	See ECN	SYT	Part number changed from previous revision. New and old part number differ by the letter “A” Modified Functional Block diagrams Modified switching waveforms Added Footnote #13 (32-Bit Vendor I.D Code changed) Added Boundary scan information Added I_{DD}, I_X and I_{SB} values in the DC Electrical Characteristics Added t_{POWER} specifications in Switching Characteristics table Removed 119 PBGA Package Changed 165 FBGA Package from BB165C (15 x 17 x 1.20 mm) to BB165 (15 x 17 x 1.40 mm) Changed 209-Lead PBGA BG209 (14 x 22 x 2.20 mm) to BB209A (14 x 22 x 1.76 mm)
*B	300131	See ECN	SYT	Removed 150 and 117 MHz Speed Bins Changed Θ_{JA} and Θ_{JC} from TBD to 25.21 and 2.58 °C/W respectively for TQFP Package on Pg # 21 Added lead-free information for 100-pin TQFP, 165 FBGA and 209 BGA Packages. Added comment of ‘Lead-free BG and BZ packages availability’ below the Ordering Information
*C	320813	See ECN	SYT	Changed H9 pin from V_{SSQ} to V_{SS} on the Pin Configuration table for 209 FBGA Changed the test condition from V_{DD} = Min. to V_{DD} = Max for V_{OL} in the Electrical Characteristics table. Replaced the TBD’s for I_{DD}, I_{SB1}, I_{SB2}, I_{SB3} and I_{SB4} to their respective values. Replaced TBD’s for Θ_{JA} and Θ_{JC} to their respective values for 165 fBGA and 209 fBGA packages on the Thermal Resistance table. Changed C_{IN},C_{CLK} and C_{IO} to 6.5, 3 and 5.5 pF from 5, 5 and 7 pF for TQFP Package. Removed “Lead-free BG and BZ packages availability” comment below the Ordering Information
*D	331551	See ECN	SYT	Modified Address Expansion balls in the pinouts for 165 FBGA and 209 BGA Packages as per JEDEC standards and updated the Pin Definitions accordingly Modified V_{OL}, V_{OH} test conditions Replaced TBD to 100 mA for I_{DDZZ} Changed C_{IN}, C_{CLK} and C_{IO} to 7, 7and 6 pF from 5, 5 and 7 pF for 165 FBGA Package. Added Industrial Temperature Grade Changed I_{SB2} and I_{SB4} from 100 and 110 mA to 120 and 135 mA respectively Updated the Ordering Information by shading and unshading MPNs as per availability

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Document Title: CY7C1441AV33/CY7C1443AV33/CY7C1447AV33 36-Mbit (1M x 36/2M x 18/512K x 72) Flow-Through SRAM Document Number: 38-05357				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*E	417547	See ECN	RXU	Converted from Preliminary to Final. Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court”. Changed I_X current value in MODE from –5 & 30 μA to –30 & 5 μA respectively and also Changed I_X current value in ZZ from –30 & 5 μA to –5 & 30 μA respectively on page# 19. Modified test condition in note# 8 from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$. Modified “Input Load” to “Input Leakage Current except ZZ and MODE” in the Electrical Characteristics Table. Replaced Package Name column with Package Diagram in the Ordering Information table. Replaced Package Diagram of 51-85050 from *A to *B Updated the Ordering Information.
*F	473650	See ECN	VKN	Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND. Changed t_{TH}, t_{TL} from 25 ns to 20 ns and t_{TDOV} from 5 ns to 10 ns in TAP AC Switching Characteristics table. Updated the Ordering Information table.
*G	2447027	See ECN	VKN/AESA	Corrected typo in the Ordering Information table Corrected typo in the CY7C1447AV33 ‘s Logic Block diagram Updated the x72 block diagram

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